

# **METHOD OF MAKING A HYBRIDE SUBSTRATE HAVING A THIN SILICON CARBIDE MEMBRANE LAYER**

## **CROSS-REFERENCE TO RELATED APPLICATIONS**

5 This application claims the priority from pending provisional patent application Serial No. 60/272,532 filed March 1, 2001 entitled LARGE AREA HYBRID SiC WAFERS, incorporated herein by reference.

## **BACKGROUND OF THE INVENTION**

### **Field of the Invention:**

10 This invention relates to the field of semiconductor substrate manufacture; i.e., a substrate on which semiconductor materials or devices can be formed.

### **Description of the Related Art:**

The present invention makes use of a separation by implantation of oxygen (SIMOX) process.

15 In accordance with this invention, a SIMOX process provides that oxygen implanter apparatus is used to create a very thin silicon dioxide ( $\text{SiO}_2$ ,  $\text{SiO}_x$ ) layer that is buried within a relatively thick silicon carbide (SiC) wafer, thereby leaving a thin membrane layer of SiC on top of the SiC wafer. For example, such oxygen implantation equipment is manufactured by Ibis Technology Corporation.

20 The present invention uses a step of etching  $\text{SiO}_2$  ( $\text{SiO}_x$ ) in hydrofluoric acid.

The present invention uses a wafer-bonding step. Wafer bonding of a variety of materials is known.

U.S. Patent 5,798,293, incorporated herein by reference, is cited for its teaching of the production of a semiconductor layer of SiC of the 3C polytype on top of a semiconductor substrate layer using a wafer-bonding technique.

5 U.S. Patent 5,877,070, incorporated herein by reference, is cited for its teaching of transferring an upper portion of a first mono-crystalline substrate to a second substrate using hydrogen trap-induced implantation of the first substrate, forming micro-cracks in the hydrogen traps, direct wafer bonding the first substrate to the second substrate, and growing the micro-cracks such that the upper portion of the first substrate separates from the first substrate.

10 U.S. Patent 5,966,620, incorporated herein by reference, is cited for its teaching of the use of the implantation of helium ions or hydrogen ions into a single crystal silicon substrate in order to form micro-cavities in the implantation region. Separation is achieved due to the fragility of the implantation region, and by the application of an external force, by oxidation of the implantation  
15 layer, or by laser heating of the implantation layer.

U.S. Patent 6,054,370, incorporated herein by reference, is cited for its teaching of the formation of first damaged regions in a substrate underneath areas wherein active devices are formed forming second damaged areas in the substrate at locations between the first damaged regions, causing a film to detach  
20 from the substrate at locations where the first and second damaged regions are formed, and transferring the film to a wafer.

U.S. Patent 6,120,597, incorporated herein by reference, is cited for its teaching of the detaching of a single crystal film from an epilayer/substrate or bulk crystal structure wherein ions are implanted into the crystal structure to  
25 form a damaged layer within the crystal structure at an implantation depth below a top surface of the crystal structure, and wherein chemical etching effects detachment of the single crystal film from the crystal structure.

### SUMMARY OF THE INVENTION

This invention provides for the fabrication of hybrid substrates wherein a thin membrane of SiC is lifted off or sliced from a relatively thick SiC wafer, and wherein the thin SiC membrane is wafer bonded to the surface of a substrate-of-choice, to thereby form a hybrid substrate that is made up of the thin  
5 membrane of SiC and the substrate-of-choice.

While the invention will be described relative to the use of a relatively thick SiC wafer within the spirit and scope of the invention such a semiconductor wafer can be selected from SiC polytypes, non-limiting examples being 6H-SiC,  
10 4H-SiC, 3C-SiC and 15R-SiC.

Use of the relatively thick and expensive SiC wafer is maximized since many thin SiC membranes can be produced from one thick SiC wafer. That is, the thick and expensive SiC wafer can be re-used to form a number of thin SiC membranes wherein the now-exposed surface of the relatively thick SiC wafer is  
15 polished before the next thin SiC membrane is removed from the thick SiC wafer.

Wafer bonding of the SiC membrane to the substrate-of-choice is performed using commercially-available substrates-of-choice. In this manner, the invention provides relatively inexpensive hybrid SiC substrates.

20 An embodiment of the invention includes a three-step process. In this three-step process, a buried SiO<sub>2</sub> layer, or more generally a SiO<sub>x</sub> layer, is first formed in a relatively thick SiC wafer by oxygen implantation at an elevated temperature thereby forming a thin SiC membrane on top of the buried SiO<sub>2</sub> layer.

25 Secondly, the exposed surface of the thin SiC membrane is wafer bonded to the surface of a substrate-of-choice; for example, to a silicon (Si), or a polycrystalline SiC substrate. Optionally, a wetting/bonding layer can be

provided between the two wafer-bonding surfaces. Non-limiting examples of such a wetting/bonding layer are layers that contain silicon, such as silicon nitride ( $\text{Si}_3\text{N}_4$ ).

5 Thirdly, the thin SiC membrane is separated from the relatively thick SiC wafer; for example, by using a hydrofluoric acid etching step to remove the buried  $\text{SiO}_2$  ( $\text{SiO}_x$ ) layer.

### BRIEF DESCRIPTION OF THE DRAWINGS

10 FIGURES 1A, 1B and 1C show a three-step process by which hybrid substrates having a thin SiC membrane are produced in accordance with the invention, wherein FIGURE 1A shows a buried  $\text{SiO}_2$  ( $\text{SiO}_x$ ) layer that is formed within a SiC wafer by oxygen implantation, thereby leaving a top disposed and thin SiC membrane, FIGURE 1B shows a substrate-of-choice that has been wafer bonded to the top and exposed surface of the thin SiC membrane, and FIGURE 1C shows that the thin SiC membrane has been lifted off, removed from, sliced from, or separated from, the top of the SiC wafer by etching SiC wafer 11 in 15 hydrofluoric acid, the result being a thin SiC membrane that is wafer bonded onto the substrate-of-choice.

FIGURE 2A shows how a number of thin and circular SiC membranes are wafer bonded onto the surface of a circular substrate of choice.

20 FIGURE 2B shows how a number of thin and hexagonally-shaped SiC membranes are wafer bonded onto the surface of a circular substrate-of-choice.

FIGURE 2C shows how a number of thin and four-sided SiC membranes are wafer bonded onto the surface of a circular substrate-of-choice.

FIGURES 3A and 3B show a method in accordance with the invention.

### DESCRIPTION OF THE PREFERRED EMBODIMENT

With reference to FIGURE 1A in accordance with the invention a buried  $\text{SiO}_2$  or  $\text{SiO}_x$  layer 10 (hereinafter  $\text{SiO}_2$ ) is formed in a SiC wafer 11 by oxygen implantation, thereby leaving a top disposed and thin SiC membrane 12 that is, for example, about one micrometer thick or less. The oxygen implantation step of FIGURE 1A is usually performed at a high temperature; for example, from about 600 to about 700 degrees centigrade.

As a feature of the invention, a thermal oxidation step may be provided, for example at a temperature about 1150 degrees centigrade and in steam (wet oxidation) or in dry oxygen (dry oxidation), in order to grow  $\text{SiO}_2$  layer 10, thereby redistributing and smoothening the bond interface that exists between  $\text{SiO}_2$  layer 10 and SiC membrane 12.

In FIGURE 1B, a substrate-of-choice 13, for example a silicon (Si) substrate 13, is wafer bonded to the top, polished, and exposed surface 14 of thin SiC membrane 12. FIGURE 1B shows an optional  $\text{Si}_3\text{N}_4$  wetting layer 15 that can be provided between the top surface 14 of thin SiC membrane 12 and the bottom surface 20 of substrate-of-choice 13 prior to wafer bonding.

As used herein, the term wafer bonding is intended to mean a method of securely bonding two materials together that may have incompatible growth and processing technologies, wherein two polished and flat surfaces of almost any material are brought into physical contact so as to be locally attracted to each other by van der Waals forces, thus resulting in the bonding of the two polished and flat surfaces. In practice, wafer-bonding processes often requires an elevated temperature, a controlled atmosphere, and an elaborate surface cleaning procedure. Usually, the wafer-bonding process is performed in a clean environment to avoid particle contamination between the two flat bonding surfaces since contamination can cause unbonded surface areas to occur. After physically contacting the two polished and flat surfaces, bonding usually begins in one surface location, typically after applying a slight pressure. The bonded

surface area then spreads laterally over the area of the two contacting surfaces within a few seconds, generally independent of wafer thickness and distance from the rim of the wafer. Compression and liquid surface tension helps the two surfaces conform to each other, thus assuring good contact even when the individual contacting surfaces are slightly non-parallel. Crystallites within the two contacting surface can fuse together at elevated temperatures due to surface energy induced migration, or due to the formation of bonds between the surface species (i.e., Si-C or Si-Si, when bonding SiC to Si). In a nonlimiting embodiment of the invention wafer-bonding was performed at a temperature of from about 500 to about 1000 degrees, in the presence of an uniaxial pressure, and in the presence of a forming gas such as a mixture of hydrogen and nitrogen.

In the process step of FIGURE 1B, the intermediate wetting/bonding layer that contains silicon ( $\text{Si}_3\text{N}_4$ ) may be provided, if desired, to improve the strength of the wafer bonding of substrate-of-choice 13 to SiC membrane 12.

In the process step of FIGURE 1C, the thin SiC membrane 12 has been lifted off, or separated from, the top of FIGURE 1A SiC wafer 11 by etching  $\text{SiO}_2$  layer 10 in hydrofluoric acid. The result is a thin SiC membrane 12 that is wafer bonded onto the surface 20 of substrate-of-choice 13. As a feature of the invention, a high temperature annealing step may be provided for the substrate assembly 12,13.

A final Chemical Mechanical Polishing (CMP) step may now be performed on the now-exposed top surface 21 of relatively thick wafer 22.

Substrate-of-choice 13 is selected in accordance with an end user application in order to optimize the electrical properties, the thermal conductivities, and/or the insulating properties of substrate-of-choice 13 in accordance with the application. Applications where this invention finds utility include large-area substrates-of-choice 13 for use in RF applications (insulating

substrates), near DC power and optical devices (conducting substrates), and for use as seeds for large-diameter boule growth. As will be appreciated, the choices for substrate-of-choice 13 can vary widely for different applications.

Substrate-of-choice 13 for SiC epitaxial growth requires mechanical  
5 stability and the ability to withstand temperatures as high as 1700°C. The use of polycrystalline SiC, sapphire, polycrystalline or crystalline AlN for applications requiring semi-insulating properties, and diamond and polycrystalline SiC for applications requiring conducting properties, are suggested for substrate-of-choice 13.

10 Substrate-of-choice 13 selections for III-V nitride growth require mechanical stability and the ability to withstand temperatures as high as 1100°C. The use of polycrystalline SiC, silicon oxide and silicon nitride for applications requiring semi-insulating properties, and silicon for applications requiring conducting properties, are suggested for substrate-of-choice 13.

15 Substrate-of-choice 13 selections for use in seeding SiC boule growth include crystalline SiC membranes bonded to polycrystalline SiC.

Substrate-of-choice 13 selections for thermal considerations include polycrystalline SiC and diamond.

There are several ways to scale the diameter 25 of substrate-of-choice 13  
20 by wafer bonding a number of thin SiC membranes 12 to each substrate-of-choice 13, as is illustrated by FIGURES 2A, 2B and 2C, wherein SiC membranes 12 are of a circular shape in FIGURE 2A, SiC membranes 12 are of a hexagonal shape in FIGURE 2B, and SiC membranes 12 are a square shape in FIGURE 2C. In these figures, the diameter 20 of substrate-of-choice 13 is, for example, about  
25 6 inches.

The present invention provides for the making of large area SiC membranes 12 that also have utility as seeds for use in boule growth. In this

utility, SiC membranes 12 can be provided that are as much as 3 times larger diameter than is available using known SiC boule seed technology. In this utility, it is desirable that membranes 12 be provided that are thicker than the above-mentioned example of about one micrometer thick or less.

5        With reference to FIGURE 1A, and in accordance with an embodiment of the invention, a 4H-SiC wafer 11 was first ion-implanted with oxygen at 1.5MeV and 700°C, thus providing a buried SiO<sub>x</sub> layer 10 that was about 1μm below the top surface 14 of the 4H-SiC wafer 11. The SiC membrane maintained good crystalline quality as was determined by the use of a Rutherford Backscattering  
10       Spectroscopy.

      Second, a highly-reproducible wafer-bonding process provided direct wafer bonding of the top surface 14 of the 4H-SiC membrane 12 to either a conducting (Si) or an insulating (SiO<sub>2</sub>) substrate-of-choice 13. A strong bond and a good electrical interface was observed at the wafer-bonded interface 30  
15       between 4H-SiC membrane 12 and substrate-of-choice 13.

      Third, an efficient acid etch lift-off process provided that thin 4H-SiC membrane 12 was separated from the remainder 22 of the 4H-SiC wafer 11, as the separated 4H-SiC membrane 12 remained bonded to the Si or SiO<sub>2</sub> substrate-of-choice 13. Good reproducibility and high yield were obtained.

20       Size scaling of the above process was demonstrated using 3C-SiC to form wafer 11 to thereby provide sizes of membrane 12 up to about 2x2 cm.

      FIGURES 3A and 3B show a method in accordance with the invention wherein in step 30 SiC wafer 11 is provided, and in step 31 SiC wafer 11 is subjected to an oxygen-implantation step to thereby form a surface located SiC  
25       membrane 12 that is located on top of a buried SiO<sub>2</sub> layer 10.

      Step 32 is an optional thermal-oxidation step that may be provided to smoothen the interface between buried SiO<sub>2</sub> layer 10 and SiC membrane 12.



Step 33 provides an optional step whereby wafer 11 and its buried SiO<sub>2</sub> layer 10 are high-temperature annealed.

Step 34 provides a substrate of choice 13, whereas step 35 optionally provides a wetting layer 15 that contains Si and is located intermediate substrate-of-choice 13 and SiC membrane 12.

Wafers 11 and substrates of choice 13 of the type that are used in accordance with this invention usually include visual indicators, for example flats or cuts, that indicate the alignment direction of the crystals that form members 13 and 11. As a feature of the invention, an optional step 36 may be provided to physically align SiC membrane 12 and substrate-of-choice 13 prior to the above-described wafer-bonding step so as to optimize the bonding of the two crystal interfaces that are provided by the two surfaces that are to be wafer bonded.

In step 37, substrate-of-choice 13 is wafer bonded to SiC membrane 12, and in step 38, the SiO<sub>2</sub> layer 10 of FIGURE 1B is removed using a hydrofluoric acid bath.

In optional step 39, the FIGURE 1C substrate assembly is annealed at a high temperature.

Relative to annealing step-33 and annealing step-39, it may be that the use of only one such step is sufficient. The utility of such a high temperature annealing step, or steps, is to repair any ion implantation induced damage that may be present within SiC membrane 12.

In step 40, the method of FIGURES 3A and 3B is repeated a number of times in order to maximize the use of the thickness of SiC wafer 11, and in order to produce a plurality of the FIGURE 1C hybrid substrates, each hybrid substrate including a substrate-of-choice 13 that is wafer bonded to a SiC membrane 12.

The invention has been described in detail while making reference to preferred embodiments thereof. However, this detailed description is not to be taken as a limitation on the spirit and scope of the invention.

What is claimed is: